Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) System comprising:

a first processor bus,

a first processor coupled to the first processor bus,

a first direct memory access unit with a first external direct memory access channel, the first direct memory access unit being coupled to the first processor bus,

a first programmable unit coupled via the first external direct memory access channel to the first direct memory access unit, said first programmable unit being programmable by the first processor,

a first shareable unit coupled to the first processor bus,

a second processor bus,

a second processor coupled to the second processor bus,

a second direct memory access unit with a second external direct memory access channel, the second direct memory access unit being coupled to the second processor bus,

a second programmable unit coupled via the second external direct memory access channel to the second direct memory access unit, said second programmable unit being programmable by the second processor, and

a second shareable unit being connected to the second processor bus,

wherein the first programmable unit and the second programmable unit each comprises a processor interface, a direct access unit core, and two external direct memory access channel interfaces,

wherein a first bi-directional communication channel is established between the first shareable unit and the second processor, and a second bi-directional communication channel is established between the second shareable unit and the first processor.

2. (original) The system of claim 1, wherein the first bi-directional communication channel and/or the second bi-directional communication channel are half-duplex channels or full-duplex channels.

3. (currently amended) The system of claim 1, wherein the first processor and the second processor are similar from an architectural point of view.

4. (currently amended) The system of claim 1, wherein the first processor and the second processor are implementations of the same type of processor design.

5. (currently amended) The system of claim 1, wherein the first processor and the second processor are implementations of different types of processor design.

6. (currently amended) The system of claim 1, wherein the first and second shareable units each comprise ~~shareable unit is~~ one of the following: a memory, a peripheral, an interface, an input device, an output device.

7. (currently amended) The system of claim 1, wherein one of the ~~two integrated processors is~~ first and second processors comprises a central processing unit, a microprocessor, a digital signal processor, a system controller, a co-processor, or an auxiliary processor.

8. (canceled)

9. (currently amended) The system of claim 1, wherein ~~the~~ each processor interface has a programming link either for connecting to a corresponding processor bus or for connecting to a corresponding processor.

10. (currently amended) The system of claim 1, wherein the first and second bi-directional communication channels are configured to transfer data and/or control information ~~is transferred~~ to and from the first and second shareable units ~~shareable unit via the communication channels~~.

11-12. (canceled)